providing a switching system having inputs and outputs;

temporarily storing data packets at an input of the switching system; and

sending only a message to an output of the switching system when each data packet arrives at the input and placing the message into a queue at the output, and, if a data packet is transmitted to a plurality of destinations, only producing a plurality of messages and placing the messages into the respective queue.--

In the Abstract:

Please replace the Abstract of the Disclosure with the new Abstract of the Disclosure, attached hereto as a separate sheet.

Remarks:

The preliminary amendment is being filed in an effort to present an application in proper U.S. format and to present claims in proper U.S. claim idiom for examination.

The newly entered claims are fully supported in the original claims.

An early action on the merits of the claims is requested.

Respectfully submitted,

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For Applicants

GLM:kc

April 19, 2001

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Marked-up Specification:

Replace the paragraph bridging pages 8 and 9 with the following:

--An access controller receives a data packet on a line (Medium Access Control MAC) from the network (LAN) and writes it via the internal bus 1 to the packet memory 44, which is likewise connected to the memory management unit 18. To match the data rate between the input and the internal bus 1, a bus access controller and a first-in-first-out memory 14 need to be provided. The respective access controller also handles the tasks associated with the transmission protocol, such as throughput control. Connected to the bus 1 are twelve access controllers for a speed of 100 megabit/s (FEMAC) and an access controller for one gigabit/s ([GEMAC] GMAC). However, only either the twelve FEMACs or the [GEMAC] GMAC are active in each case. Hence, all the units connected to the bus 1 perceive no difference as to whether the data arrives via the [GEMAC] GMAC or the FEMAC. The result of this is considerable simplification.--.

Replace the paragraph bridging pages 9 and 10 with the following:

--In the case of the [GEMAC] GMAC, the request for an appropriate data packet for a FIFO memory 20 takes too long to utilize the transmission speed of the [GEMAC] GMAC on the line fully. In this case, all twelve transmit FIFO memories 20

request and assemble frames in parallel. After assembly, the data packets are forwarded to the [GEMAC] GMAC in the correct sequence and are transmitted onto the GIGABIT Ethernet line by the [GEMAC] GMAC.--.